WHAT IS CLAIMED IS:

1. A test system which performs electrical tests on semiconductor chips formed on a semiconductor wafer, comprising:

a probe card which is provided with conductive needles in alignment with the placement of electrode pads in the semiconductor chips and connected to a test circuit;

a test circuit which is placed on said probe card and conducts tests on the semiconductor chips, based on a program; and

a control device which writes a program in said test circuit and stores therein a test result outputted from said test circuit.

2. A test system which conducts electrical tests on semiconductor chips formed on a semiconductor wafer, comprising:

a test circuit which conducts tests on the semiconductor chips formed in arbitrary positions of the semiconductor wafer;

a probing module having test wirings formed therein, which connect the semiconductor chips and said test circuit; and

a power supply device which supplies power to said each semiconductor chip and said test circuit through

said probing module.

3. A test system which performs electrical tests on semiconductor chips formed on a semiconductor wafer, comprising:

a test circuit which is formed in a scribe area or a chip area in the semiconductor wafer and tests the semiconductor chips; and

test wirings which are formed in the scribe area or a test wiring layer in the semiconductor wafer and connect said test circuit to the semiconductor chips.

4. The test system according to claim 1, wherein said test circuit includes an FPGA or a microcomputer device.

5. The test system according to claim 2, wherein said test circuit includes an FPGA or a microcomputer device.

6. The test system according to claim 3, wherein said test circuit includes an FPGA or a microcomputer device.

7. The test system according to claim 5, wherein said test circuit conducts tests on a plurality of semiconductor chips formed on a semiconductor wafer.

8. The test system according to claim 6, wherein said test circuit conducts tests on a plurality of semiconductor chips formed on a semiconductor wafer.

9. A method of generating a test program, comprising the following steps of:

describing functions set every blocks in a tester for conducting electrical tests on semiconductor chips formed on a semiconductor wafer and a function of said each semiconductor chip to be tested, in hardware description language;

inputting said hardware description and a test program to a hardware emulator;

performing simulation by the hardware emulator; and

debugging the test program.

10. A method of manufacturing a semiconductor integrated circuit device, comprising the following steps of:

forming a plurality of semiconductor chips each having a desired function on a semiconductor wafer;

placing a test circuit connected to needles and operated in accordance with a program to test said each semiconductor chip, on a probe substrate having a size corresponding to the semiconductor wafer and having the conductive needles formed thereon in alignment with the

placement of electrode pads on the semiconductor chips;

superimposing the probe substrate on the semiconductor wafer in such a manner that the needles are brought into contact with the corresponding electrode pads of the semiconductor chips;

testing said each semiconductor chip by the test circuit; and

selecting a semiconductor chip judged to be non-defective, as a product according to the test.

11. The method according to claim 6, wherein programmable logic ICs capable of configuring arbitrary logic are provided on the probe substrate in association with the respective semiconductor chips on the wafer, and the test circuit is configured within said each programmable logic IC based on the design data for said each semiconductor chip, which is described in hardware description language, and said each semiconductor chip is tested by the test circuit.

12. The method according to claim 11, wherein said test circuit is a test signal generating circuit configured so as to generate a test signal to each semiconductor chip to be tested in accordance with a predetermined algorithm.

13. The method according to claim 12, wherein said

test signal generating circuit includes a memory which holds a program therein, a controller which decodes an instruction for the program to thereby generate a control signal, and a signal generator which generates a signal to be outputted.

14. The method according to claim 13, wherein said memory is a rewritable memory.

15. The method according to claim 13, wherein said test signal generating circuit further includes timing generating means which generates a desired timing signal in response to a clock signal defined as the reference and control data outputted from memory means for holding control data about timing.

16. The method according to claim 15, wherein said memory means is a rewritable memory.

17. A method of manufacturing a semiconductor integrated circuit device, comprising the following steps of:

forming a test circuit module which is operated in accordance with a program and tests each of a plurality of semiconductor chips, on a semiconductor wafer on which said plurality of semiconductor chips are formed;

supplying a source voltage to at least said test

circuit module from the outside to thereby test said each semiconductor chip on the semiconductor wafer by said test circuit module; and

selecting the semiconductor chip judged to be non-defective by said test, as a product.

18. The method according to claim 17, wherein connections between said test circuit module and semiconductor chips to be tested are carried out by probe means which has a size corresponding to the wafer with the semiconductor chips formed thereon and which is provided with conductive needles aligned with the placement of the test circuit module and electrode pads of the semiconductor chips, and wirings which connect between the predetermined needles.

19. The method according to claim 17, wherein the connections between said test circuit module and the semiconductor chips to be tested are carried out by wirings formed in a scribe area of the wafer or a test-dedicated wiring layer.

20. The method according to claim 19, wherein the test wirings for connecting between said test circuit module and the semiconductor chips to be tested are wirings formed within the scribe area of the wafer so as to meander.

21. The method according to claim 17, wherein the test on said each semiconductor chip by said test circuit module is carried out during burn-in or aging processing.

22. The method according to claim 17, further comprising the steps of:

describing the function of said each semiconductor chip to be tested in hardware description language, inputting the hardware description and a test program to a hardware emulator, and simulating the same by the hardware emulator, thereby performing verification thereof;

thereafter converting the hardware description to design data of a logic gate level and generating layout design data of a device level for said each tested semiconductor chip, based on the design data;

extracting a test function, based on the data used in the simulation, describing the test function in hardware description language, converting the description to design data of a logic gate level, and generating layout design data of a device level of said test circuit module, based on the design data;

fabricating a wafer mask by using the layout design data of the device level for said each tested semiconductor chip and the layout design data of the device level for the test circuit module; and

forming said tested semiconductor chip and said test circuit module on one wafer by using the mask.

23. The method according to claim 17, wherein said test circuit module generates test signals supplied to a plurality of the semiconductor chips placed therearound.

24. The method according to claim 17, wherein said test circuit module tests the plurality of semiconductor chips on the semiconductor wafer.